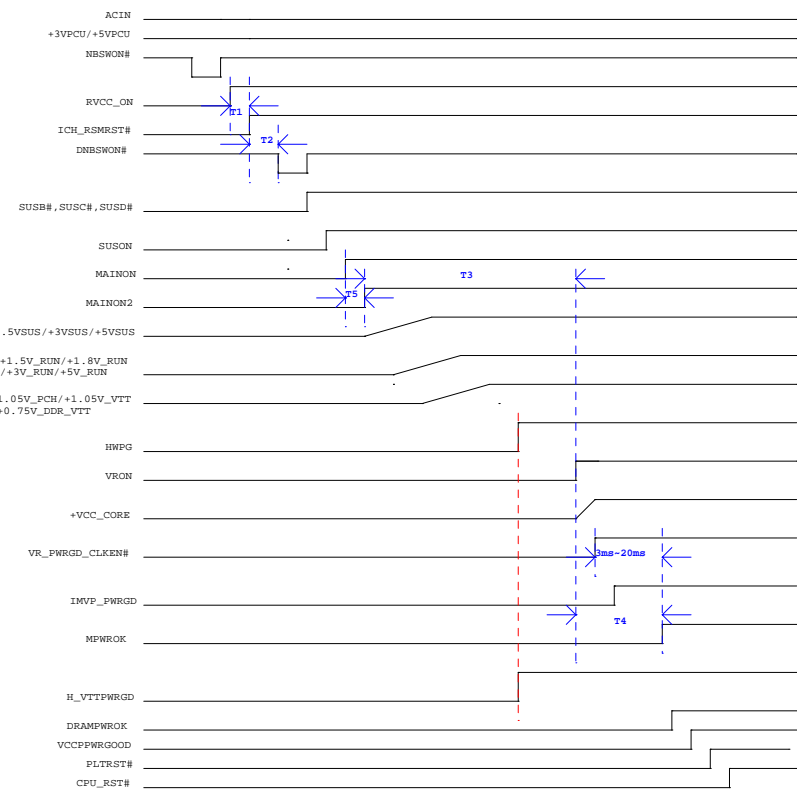


PAGE	DESCRIPTION
01	Schematic Block Diagram
02	Front Page
03	Clock Generator
04-07	Arrandale
08-13	Ibex Peak-M
14-15	DDRIII SO-DIMM(204P)
16-22	Madison
23	LCD/CCD
24	CRT/HDMI CONN
25	Card Reader (RTS5159)
26	GLAN RTL8111E-GR/J45
27	HDD/ODD/HOLE
28	USB/BLUE TOOTH
29	MINI-Card (WLAN)
30	KB/TOUCH PAD/LED
31	CODEC (ALC269)
32	EC ITE8502
33	FAN/SW/NEWCARD
34	+5V/+3V (RT8206B)
35	+1.05V/+1.8V (RT8204C)
36	CPU Core (ADP3212)
37	+1.05V_VTT (VT358)
38	DIS_GFX_VCC (MAX8792)
39	DDR3 (RT8207)
40	GFX_IO_VCC
41	DISCHARGE/3VS5/5VS5/LAN
42	CHARGER (ISL88731)
43	Clock Distribution
44	Power Tree
45	SMBUS Address
46	Change History

**System Power Sequence**

T1: RVCCON TO RSMRST# = 30ms (spec:mini 10ms)

T2: RSMRST# TO-DNBSWON = 110ms (spec:mini 100ms)

T3: MAINON2 TO VRON = 110ms (spec:mini 99ms)

T4: VRON TO MPWROK = 10ms (HWPG NEED TO BE HIGH at that time)

Note: IMVP\_CLK\_EN# (inverted) assertion to SYS\_PWROK/PCH\_PWROK assertion.  
SPEC:3ms-20ms

T5: MAINON2 to MAINON2 =500us

**Madison VGA Power Sequence**

Note1:VDDR3 should ramp-up before or simultaneously with VDDC.

Note2:For LVDS, DPx\_VDD10 should ramp-up before DPx\_VDD18

Note3:All the ASIC supplies must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence.

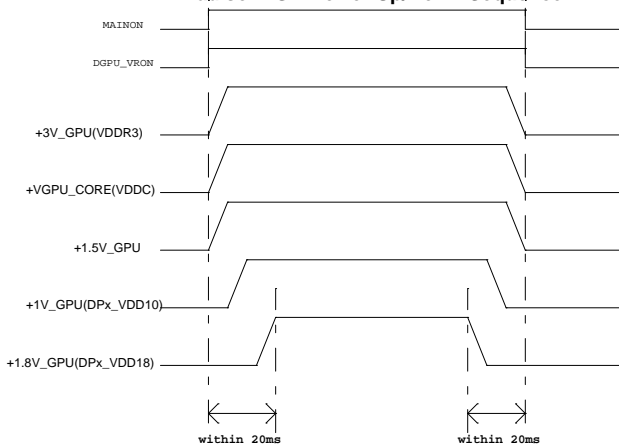
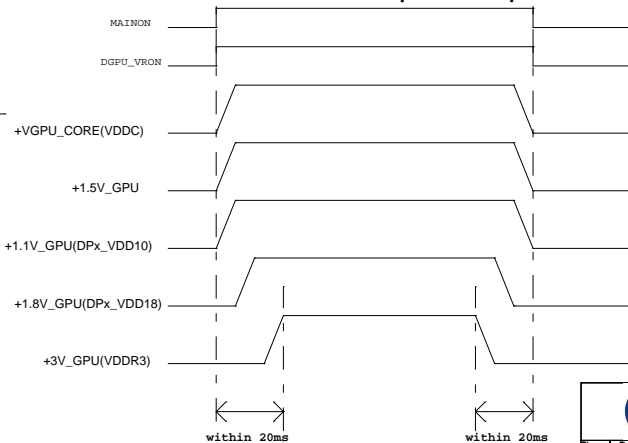
**M96 VGA Power Sequence**

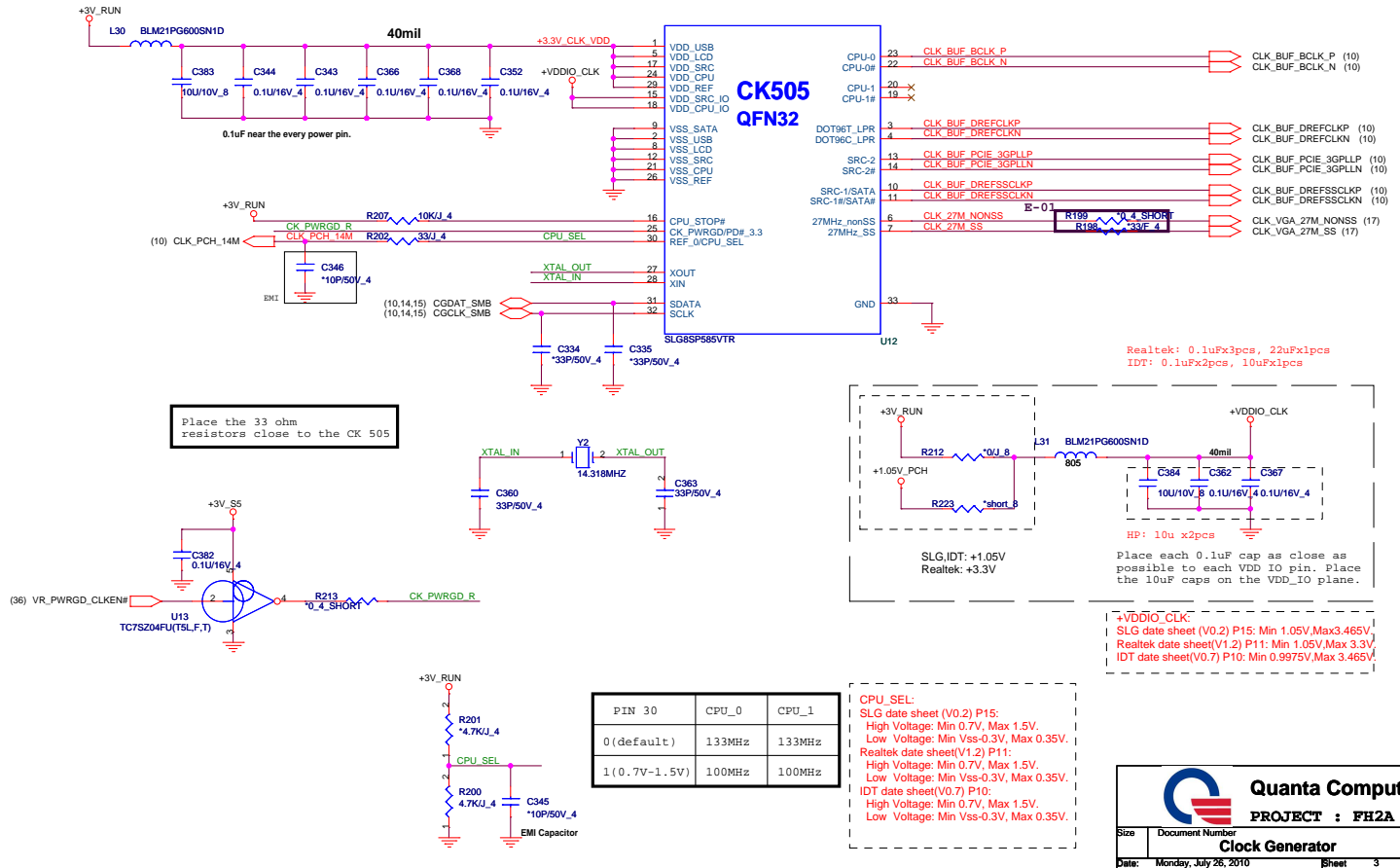
Note1:BBP must ramp up before or at the same time as VDDC but not after

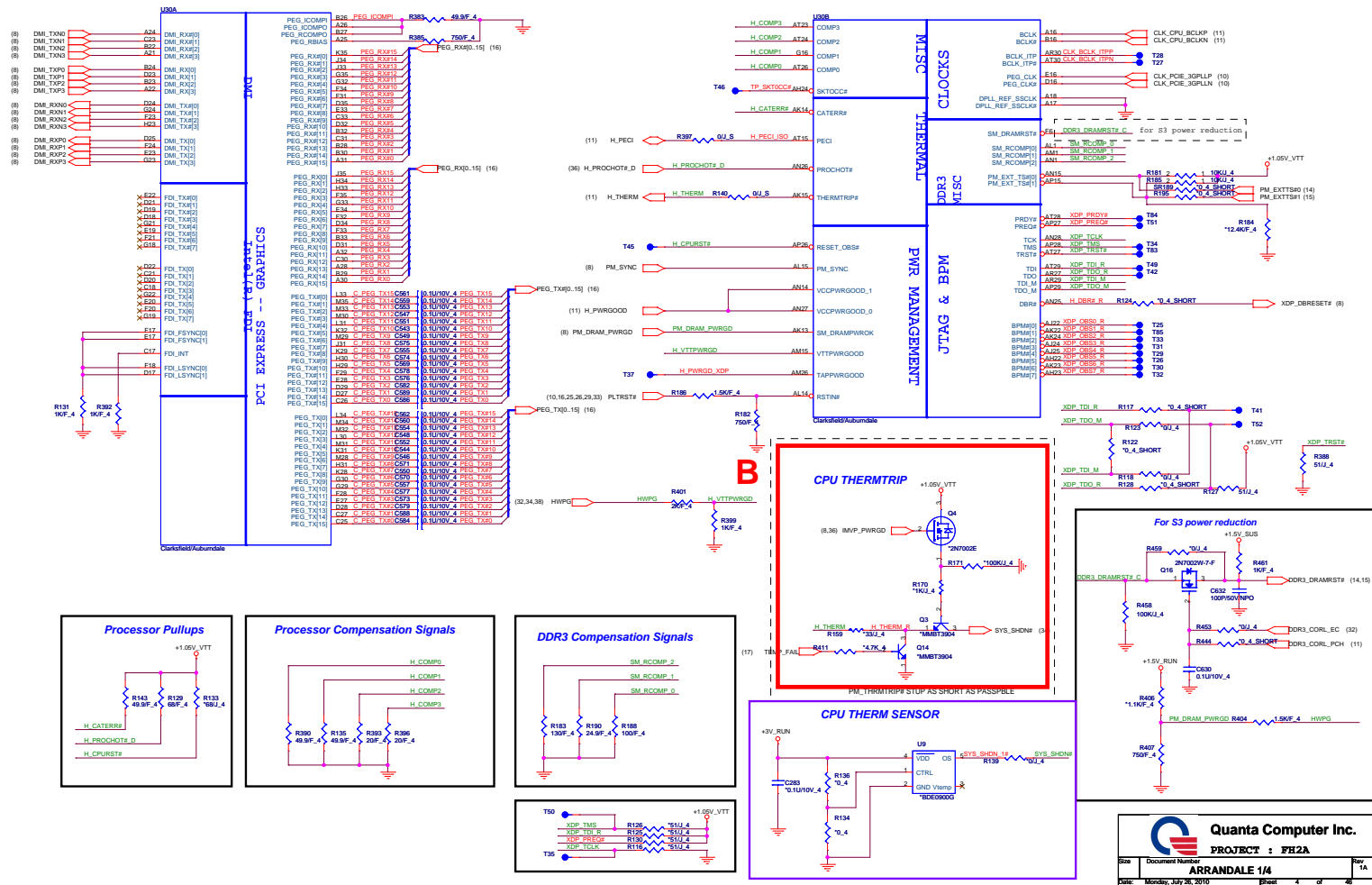
Note2:1.8-V rails should ramp before the 3.3-V rails.

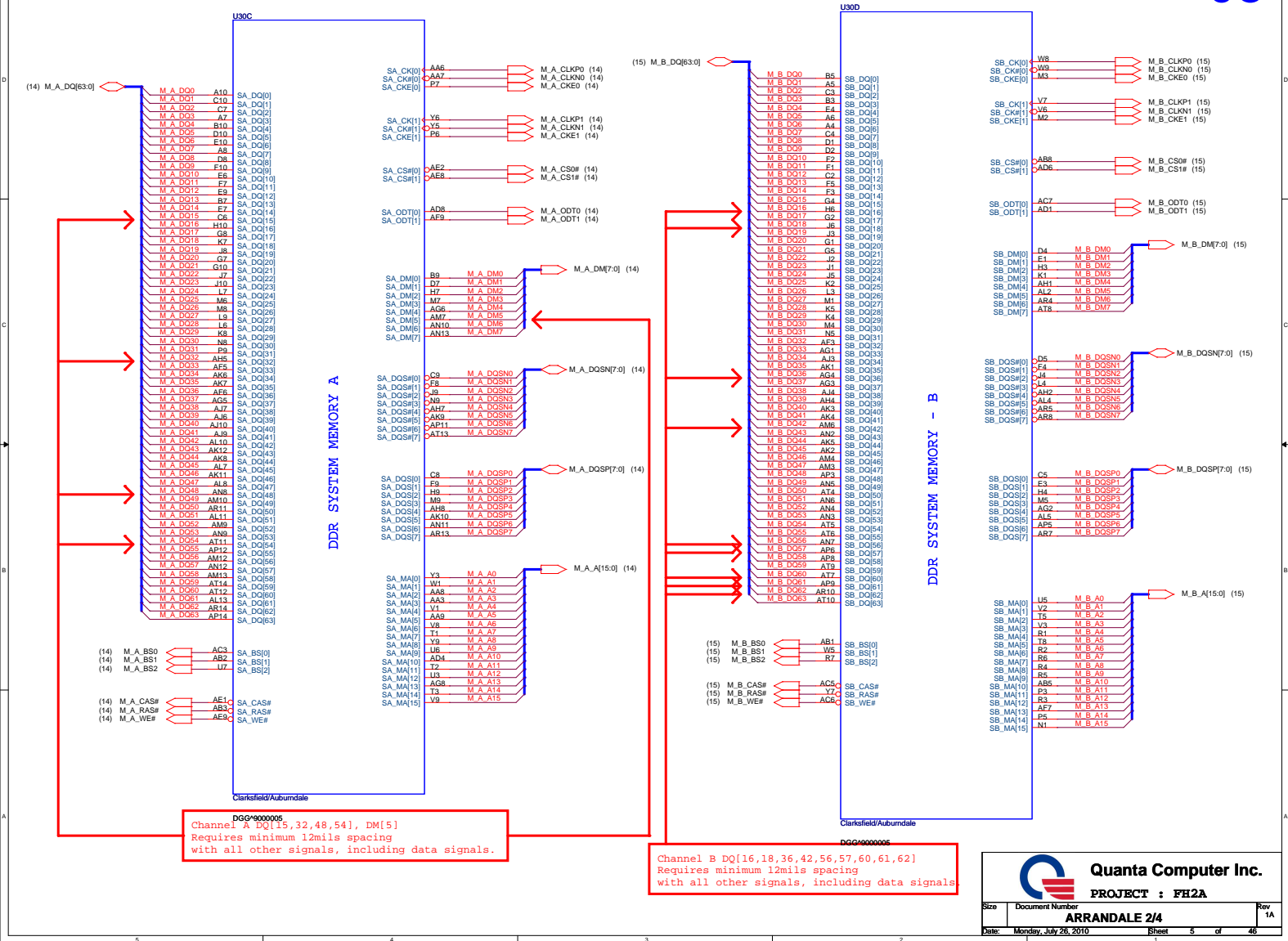
Note3:VDDC must ramp before DPx\_VDD10, DPx\_VDD18 and DPx\_PVDD.

Note4:All the ASIC supplies must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence.

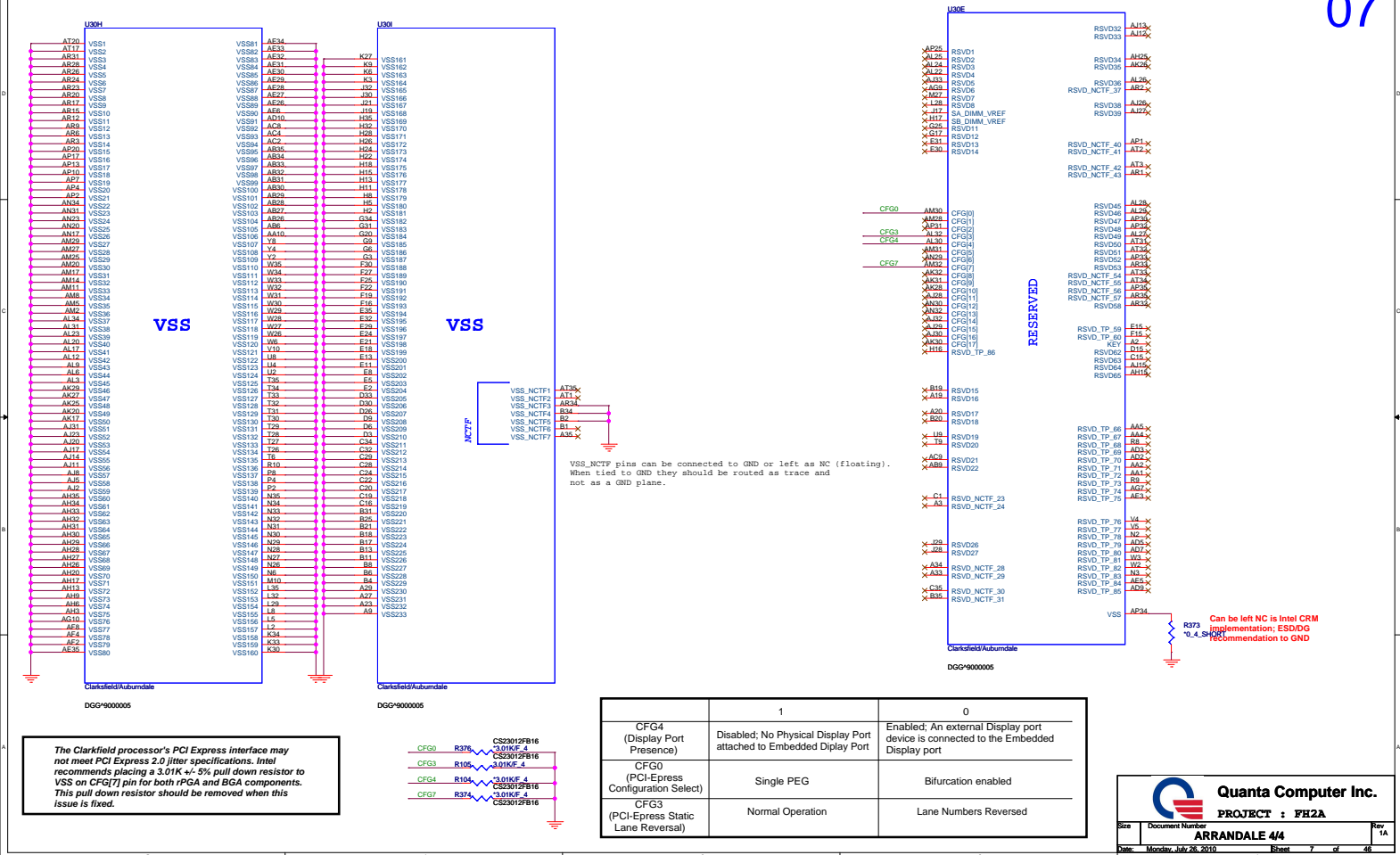
**MadisonVGA Power Up/Down Sequence****M96 VGA Power Up/Down Sequence**

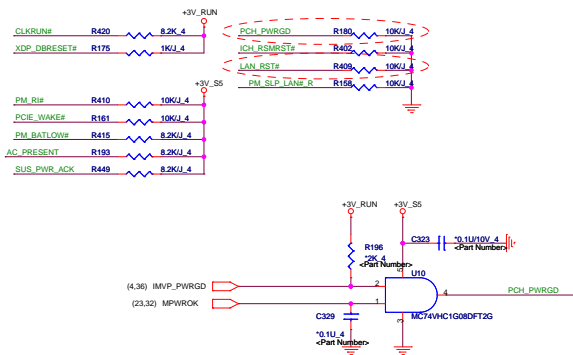
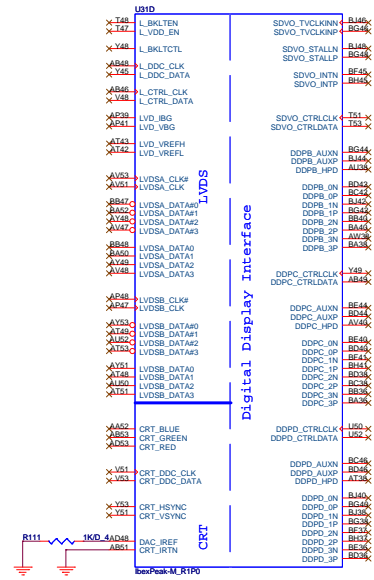










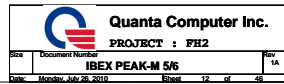




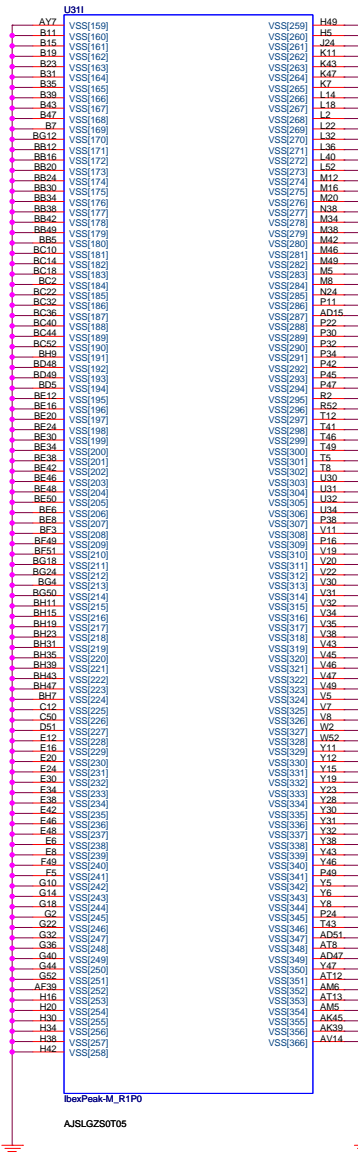
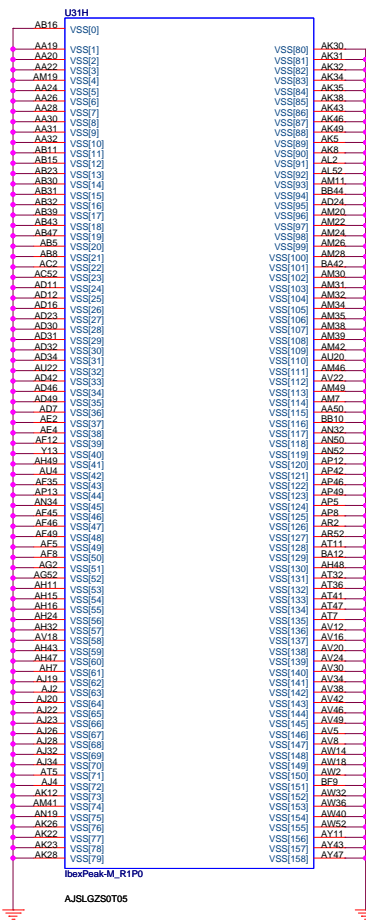








## IBEX PEAK-M (GND)

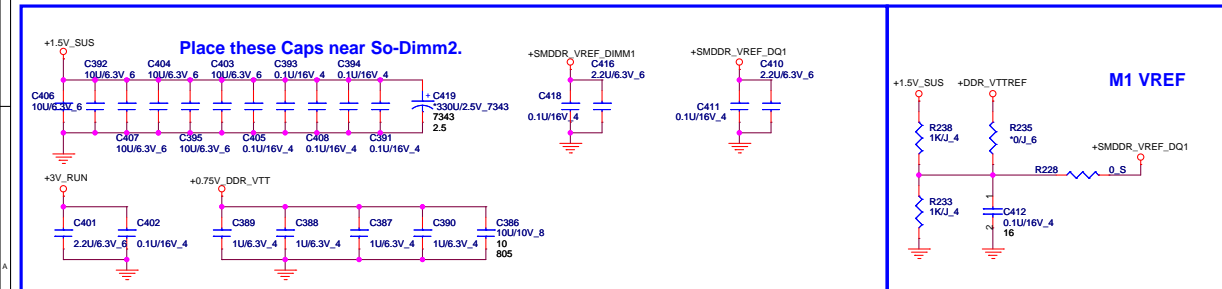
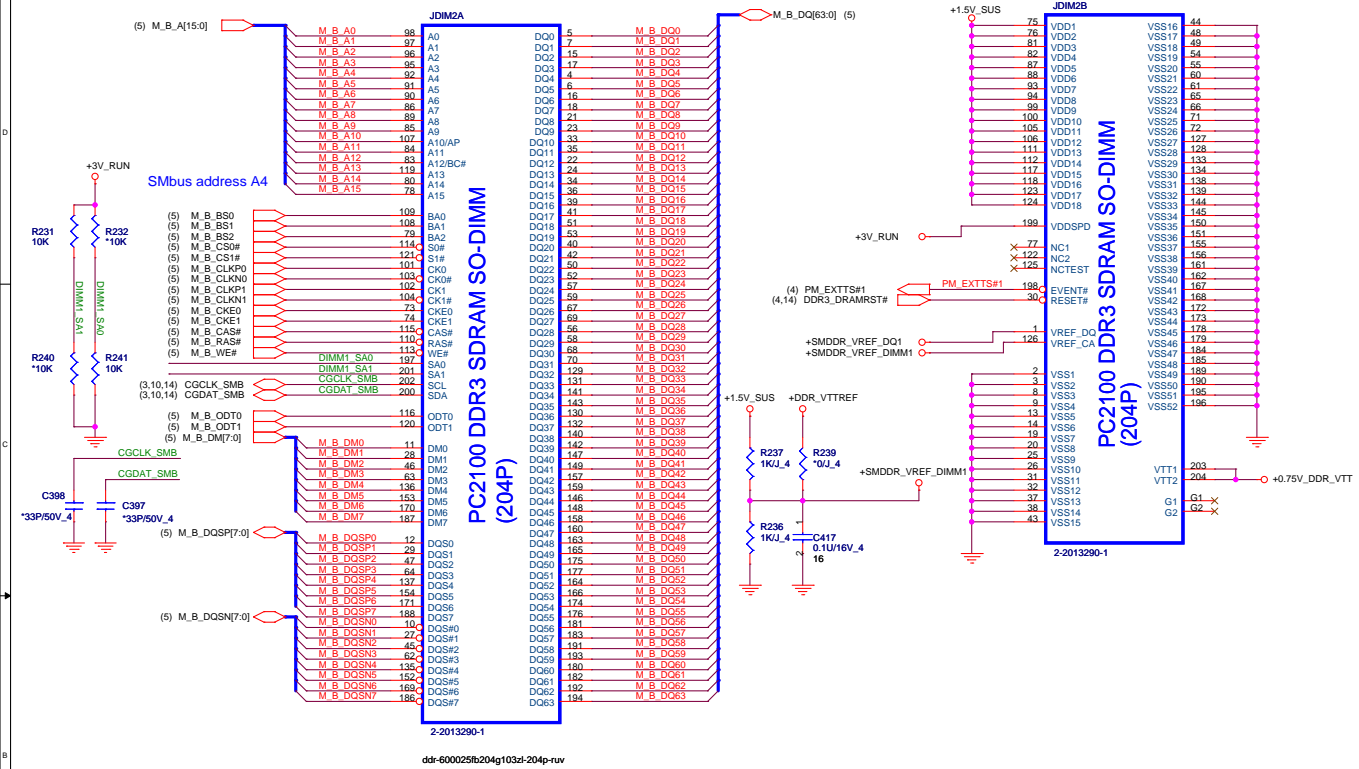


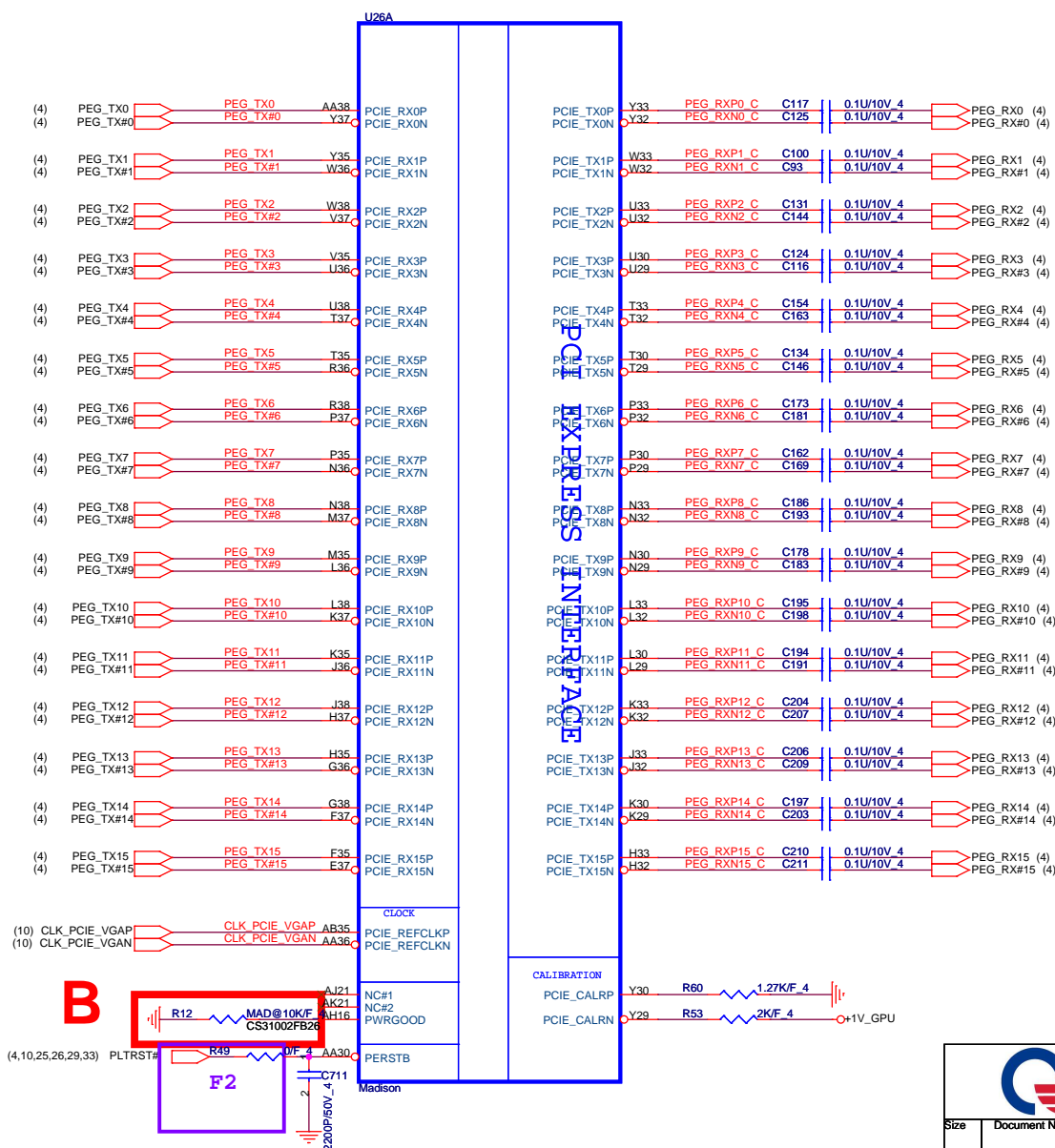
**Quanta Computer Inc.**  
PROJECT : FH2A

Size	Document Number	Rev
	IBEX PEAK-M 6/6	1A

Date: Monday, July 26, 2010 Sheet 13 of 46





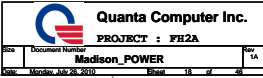


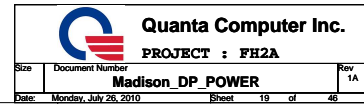
**Quanta Computer Inc.**  
PROJECT : FH2A

Size	Document Number	Rev
	Madison PCIE I/F	1A
Date:	Monday, July 26, 2010	Sheet 16 of 46

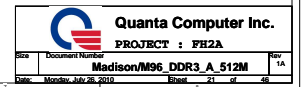


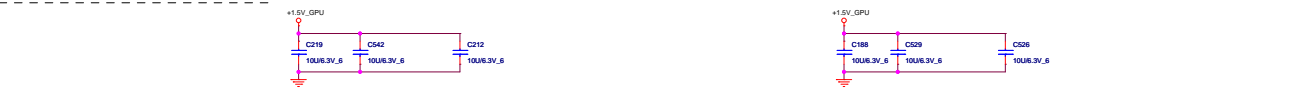
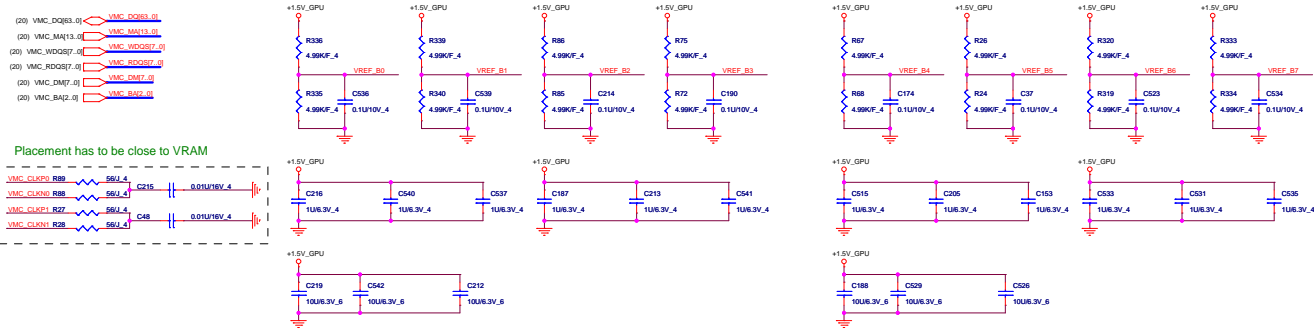




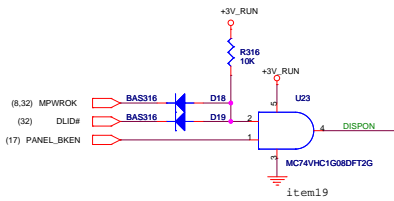




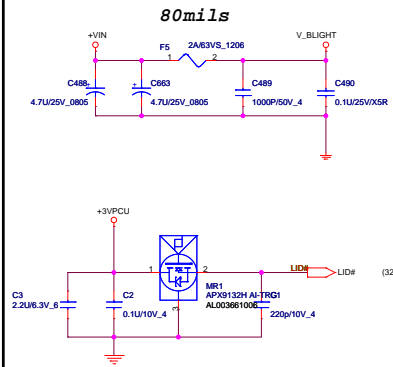




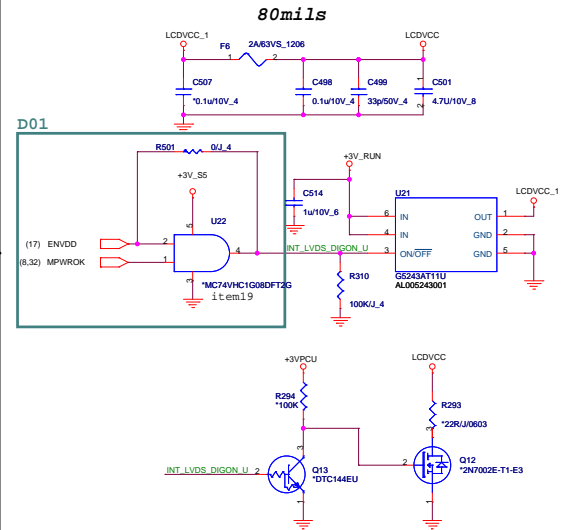
## Backlight Control(LDS)



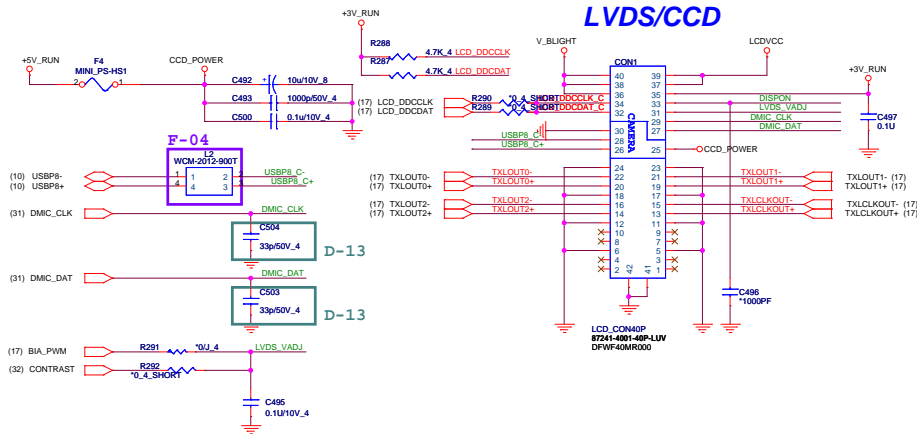
## BACKLIGHT POWER




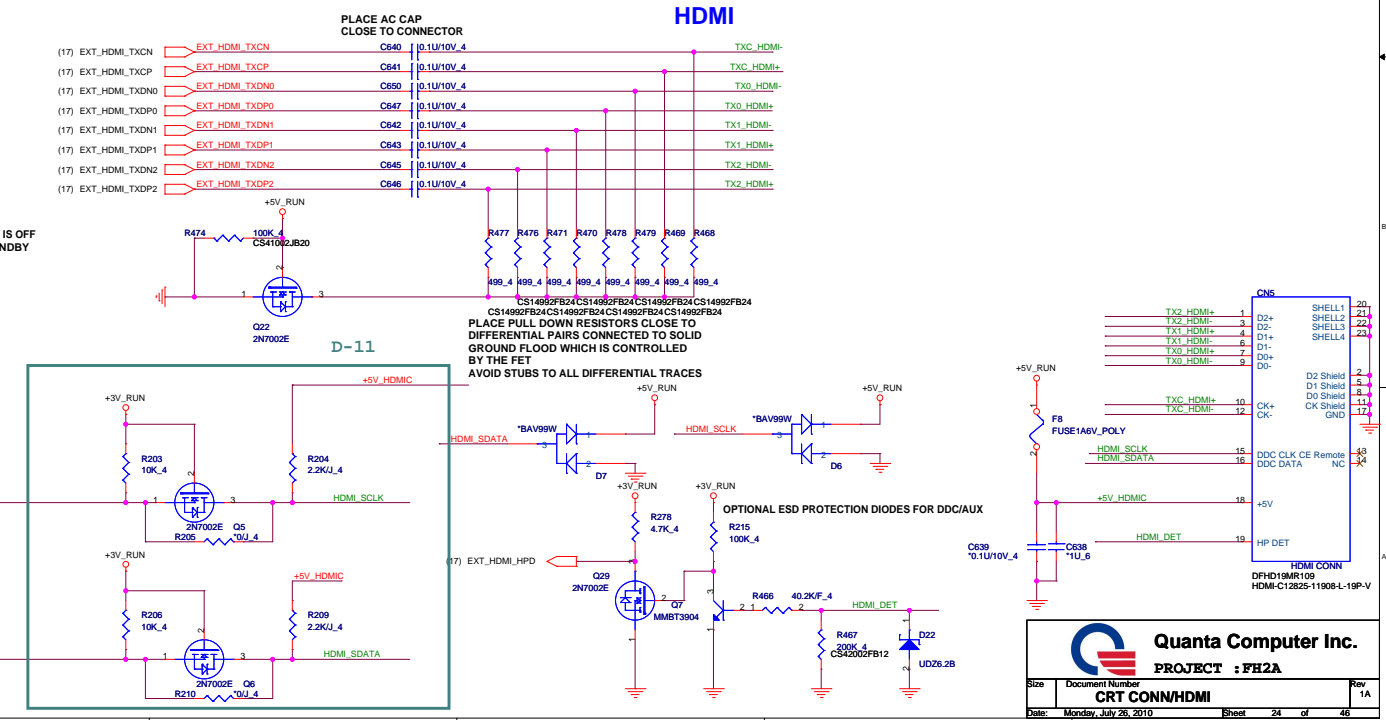
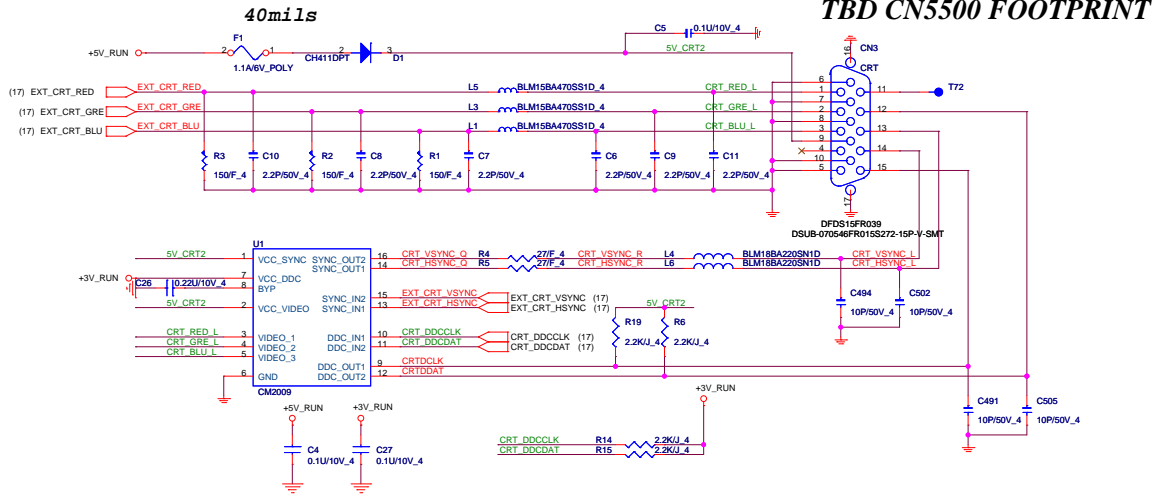
## LED Panel POWER SWITCH(LVDS)23



## LVDS/CCD

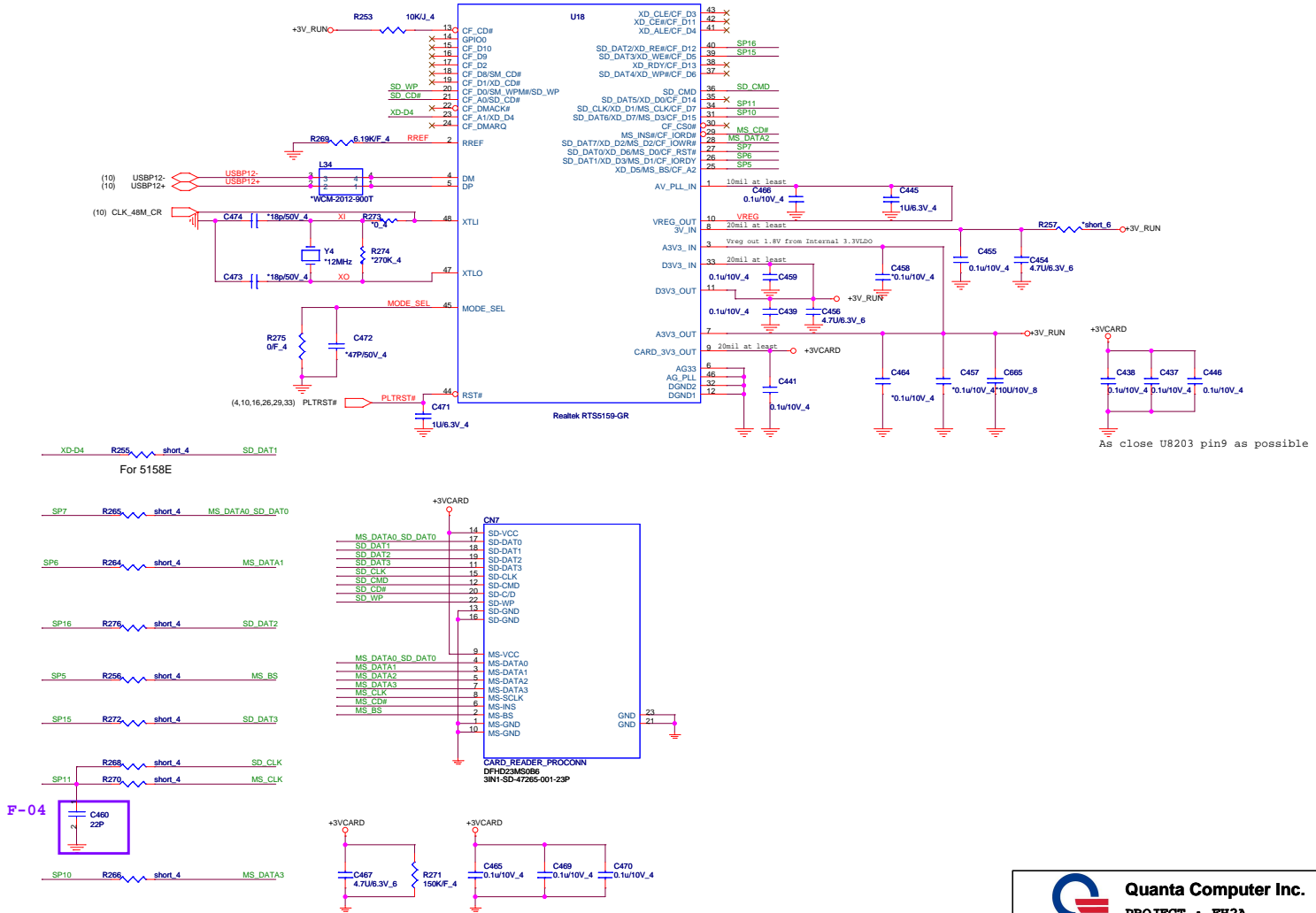


 <b>Quanta Computer Inc.</b> PROJECT : FH2A			
Size	Document Number	LCD/LED Panel/CCD	Rev 1A
Date	Monday, July 28, 2010	Sheet 23 of 46	

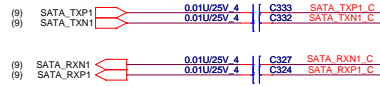
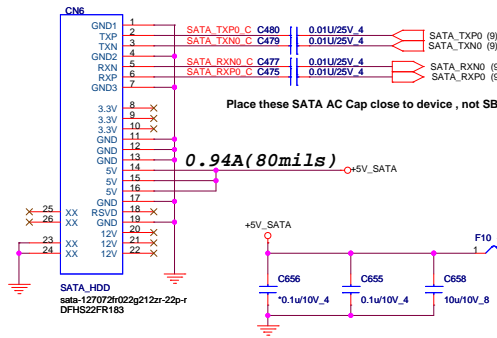




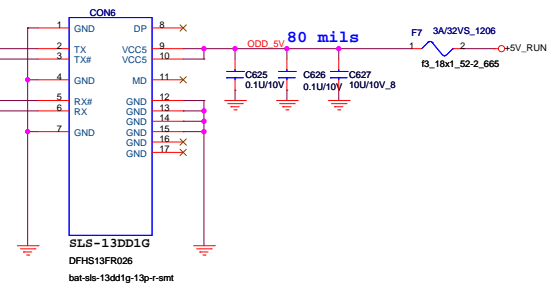
### Card Reader



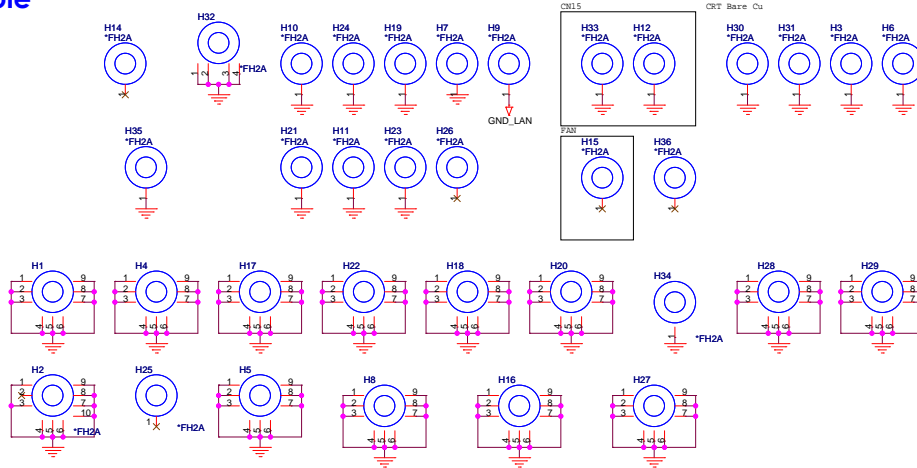




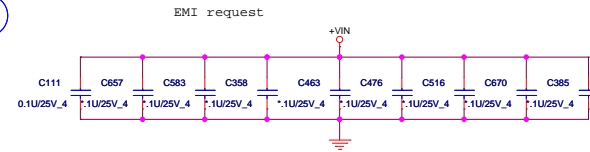
## ODD CONN



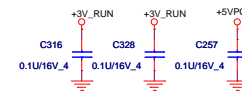
## Hole



## Decoupling Cap

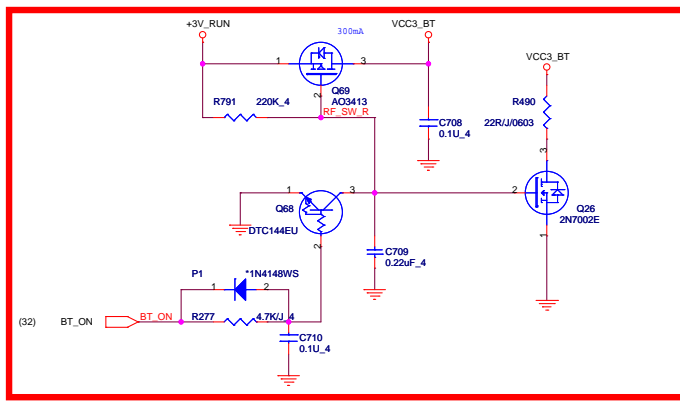


## EMI(Decoupling Cap)



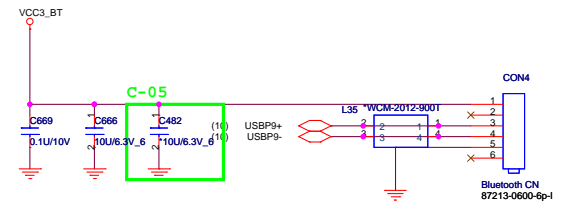
Quanta Computer Inc.			
PROJECT : FH2A			
Size	Document Number	HDD/ ODD/HOLE	Rev 1A
Date	Monday, July 26, 2010	Sheet 27 of 46	

B

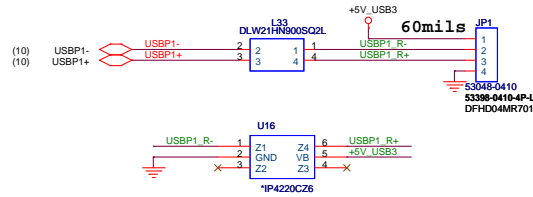
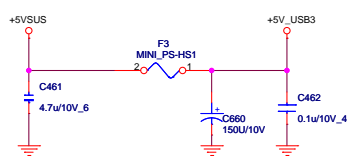
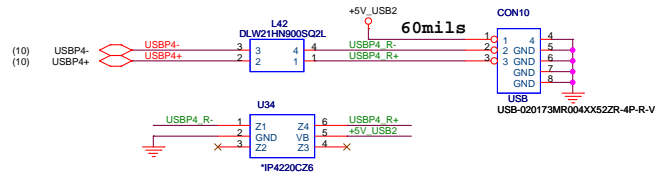
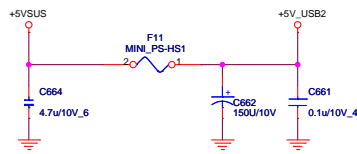
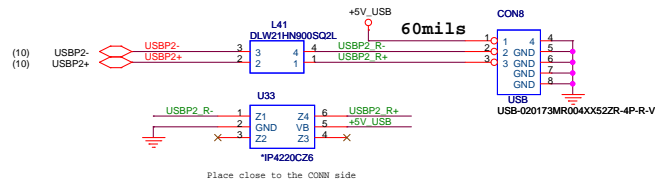
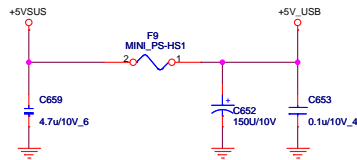



BuleTooth (BTM)

28

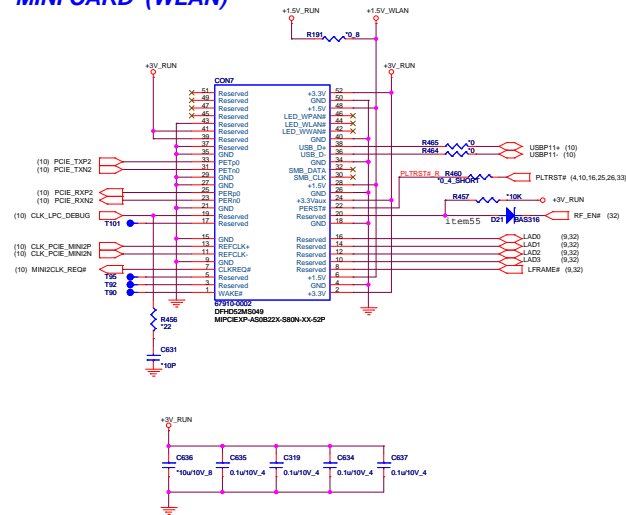


## USB Connector

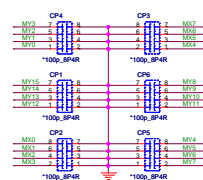
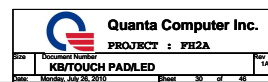


 <b>Quanta Computer Inc.</b> <b>PROJECT : FH2A</b>		
Size	Document Number	Rev
	<b>USB/BLUE TOOTH</b>	1A
Date: Monday, July 26, 2010	Sheet 28 of 46	

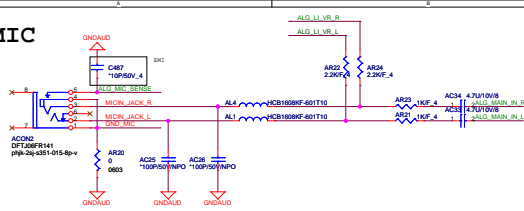
# MINI CARD (WLAN)



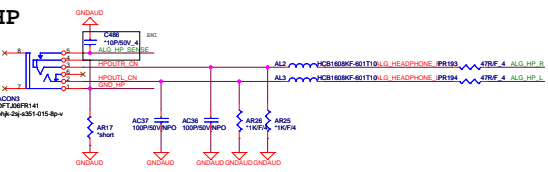
For EMI Reserve Caps for debug

[illegible]

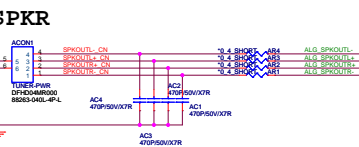
## MIC



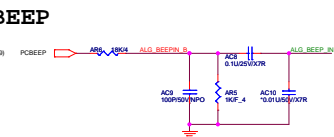
## HP



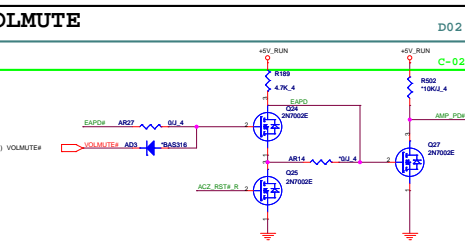
## SPKR



## BEEP

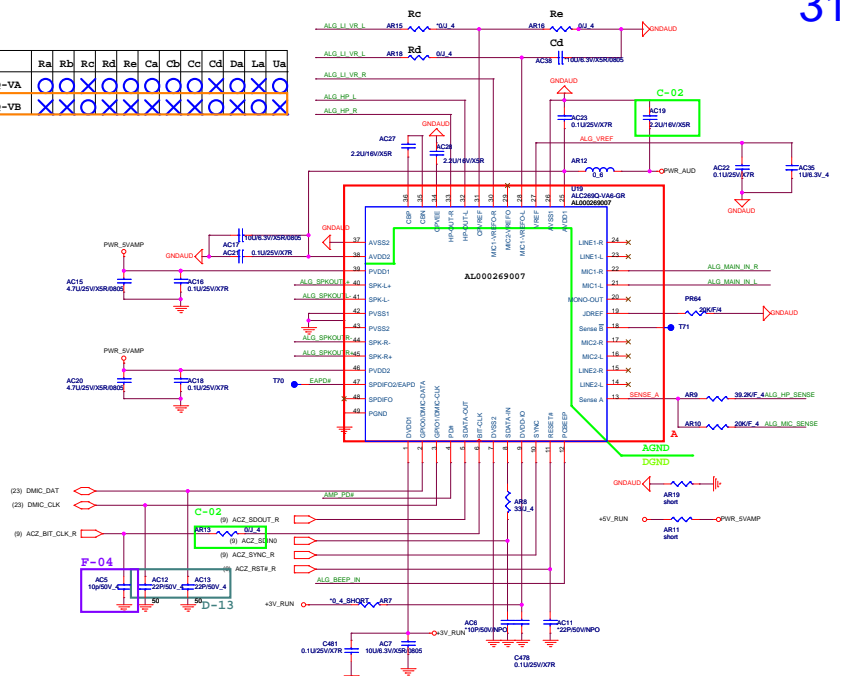


## VOLMUTE



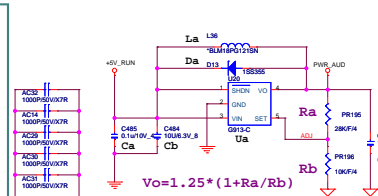
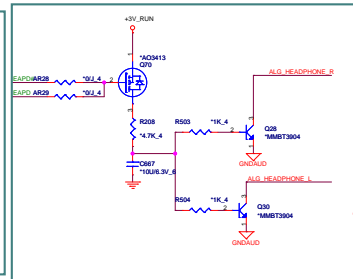
U23	Ra	Rb	Rc	Rd	Re	Cb	Cc	Cd	La	La	La
ALC269Q-VA	X	X	X	X	X	X	X	X	X	X	X
ALC269Q-VB	X	X	X	X	X	X	X	X	X	X	X

## Codec ALC269



D02

D14

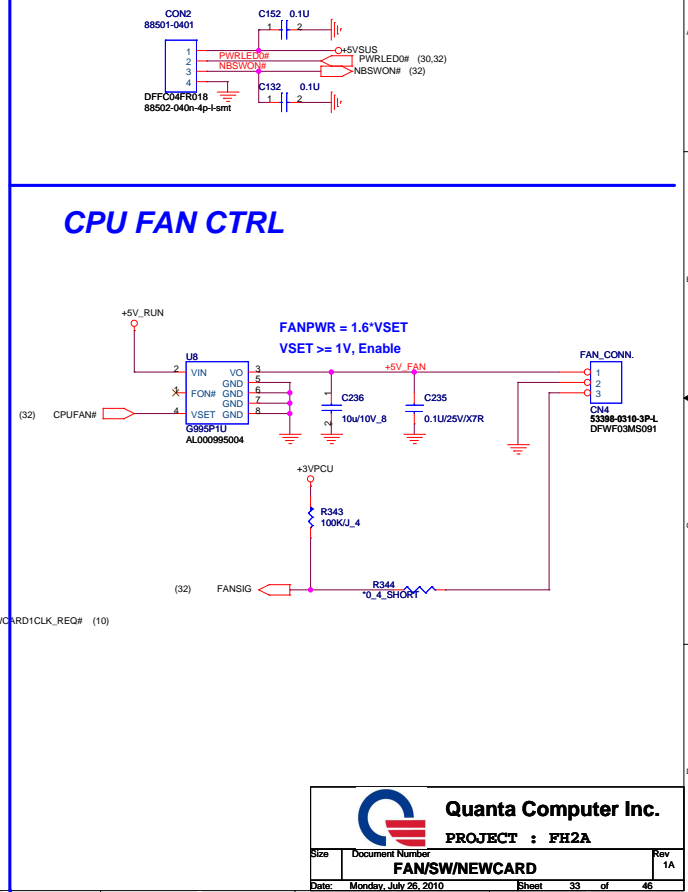


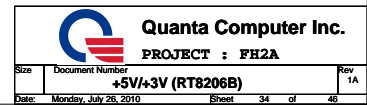
$$V_o = 1.25 * (1 + R_a / R_b)$$

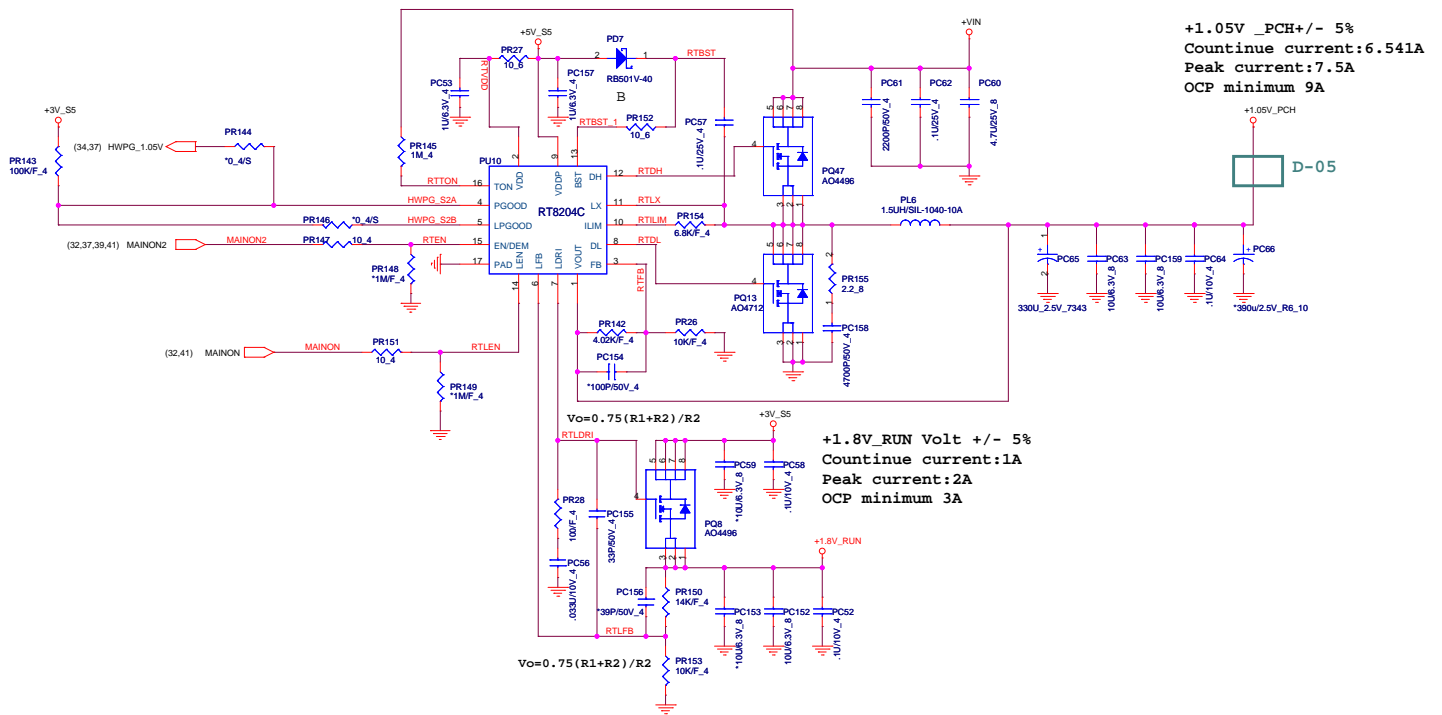





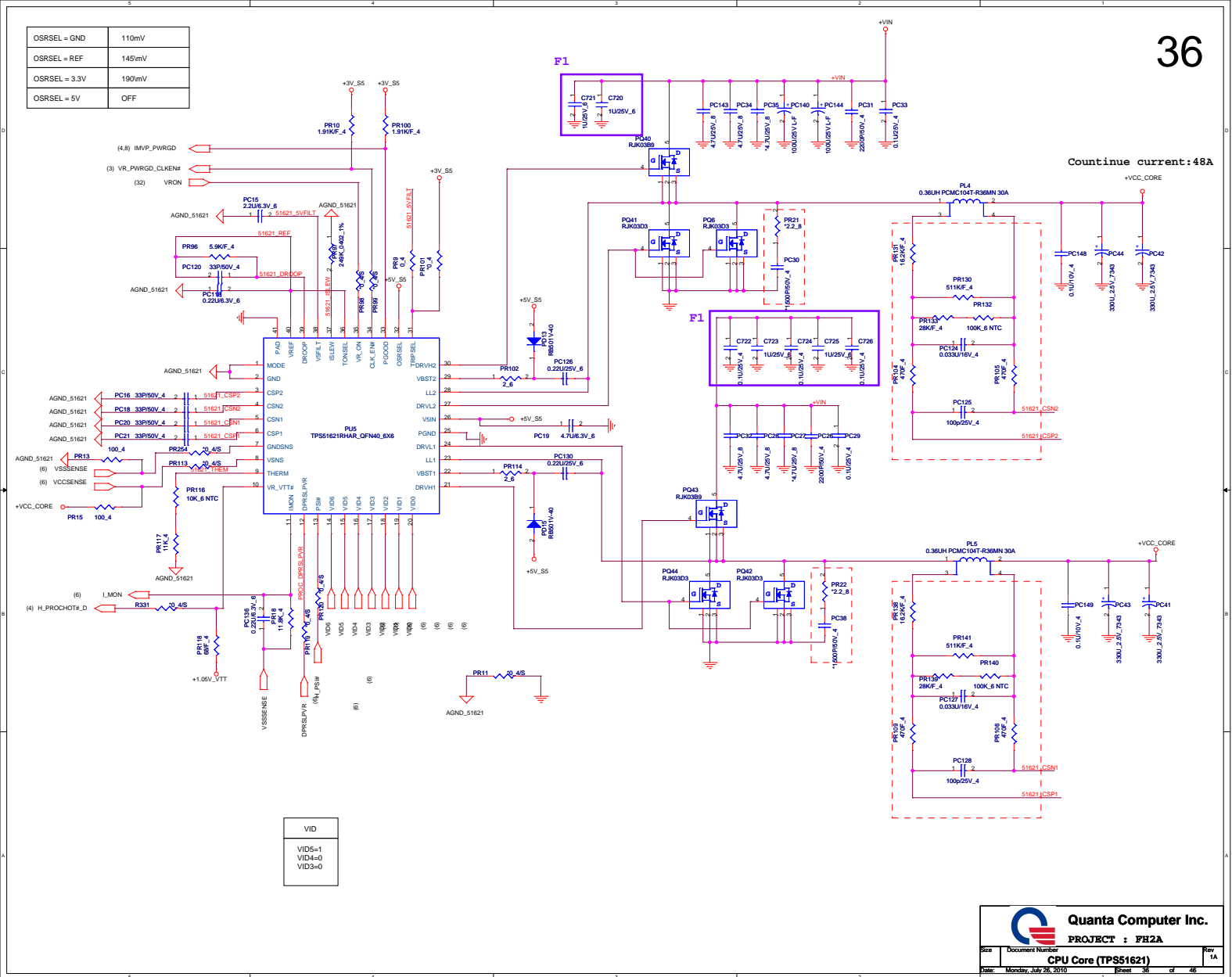
## 33

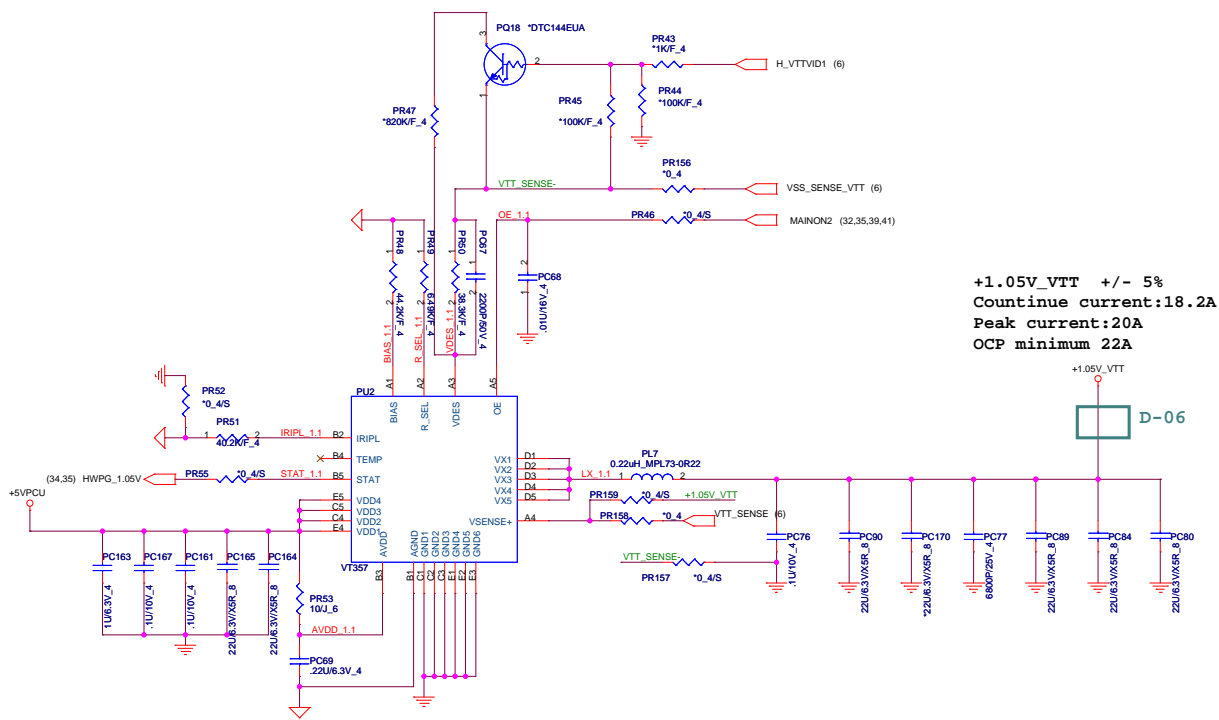




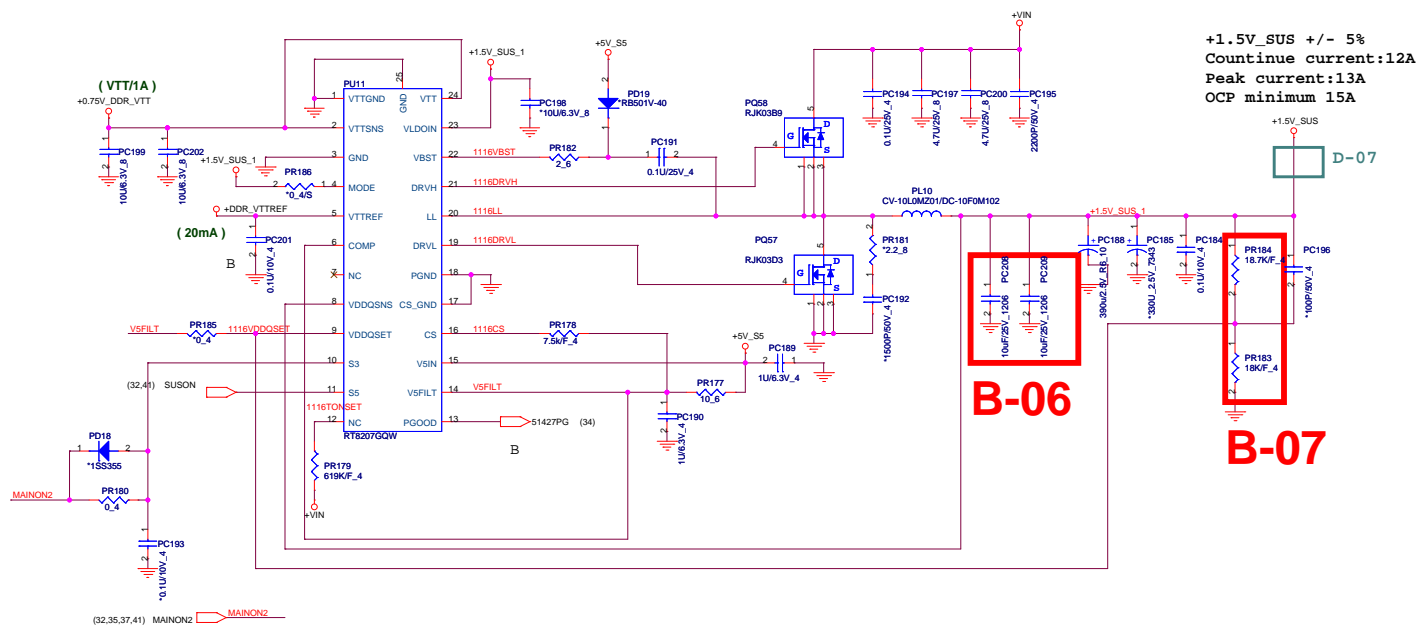


 <b>Quanta Computer Inc.</b> <b>PROJECT : FH2A</b>		
Size	Document Number	Rev
	<b>+1.05V/+1.8V (RT8204C)</b>	1A
Date:	Monday, July 26, 2010	Sheet 35 of 46

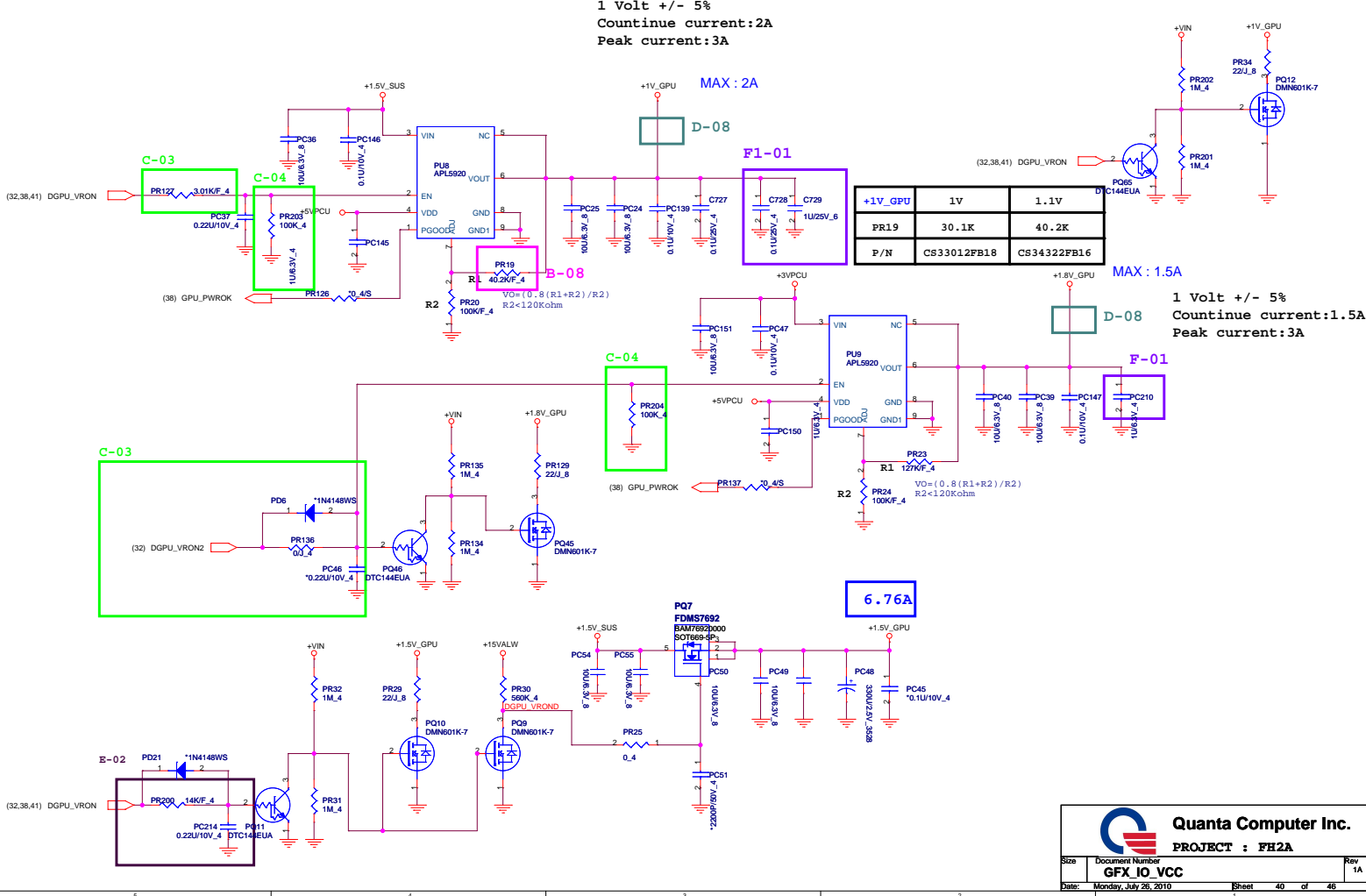




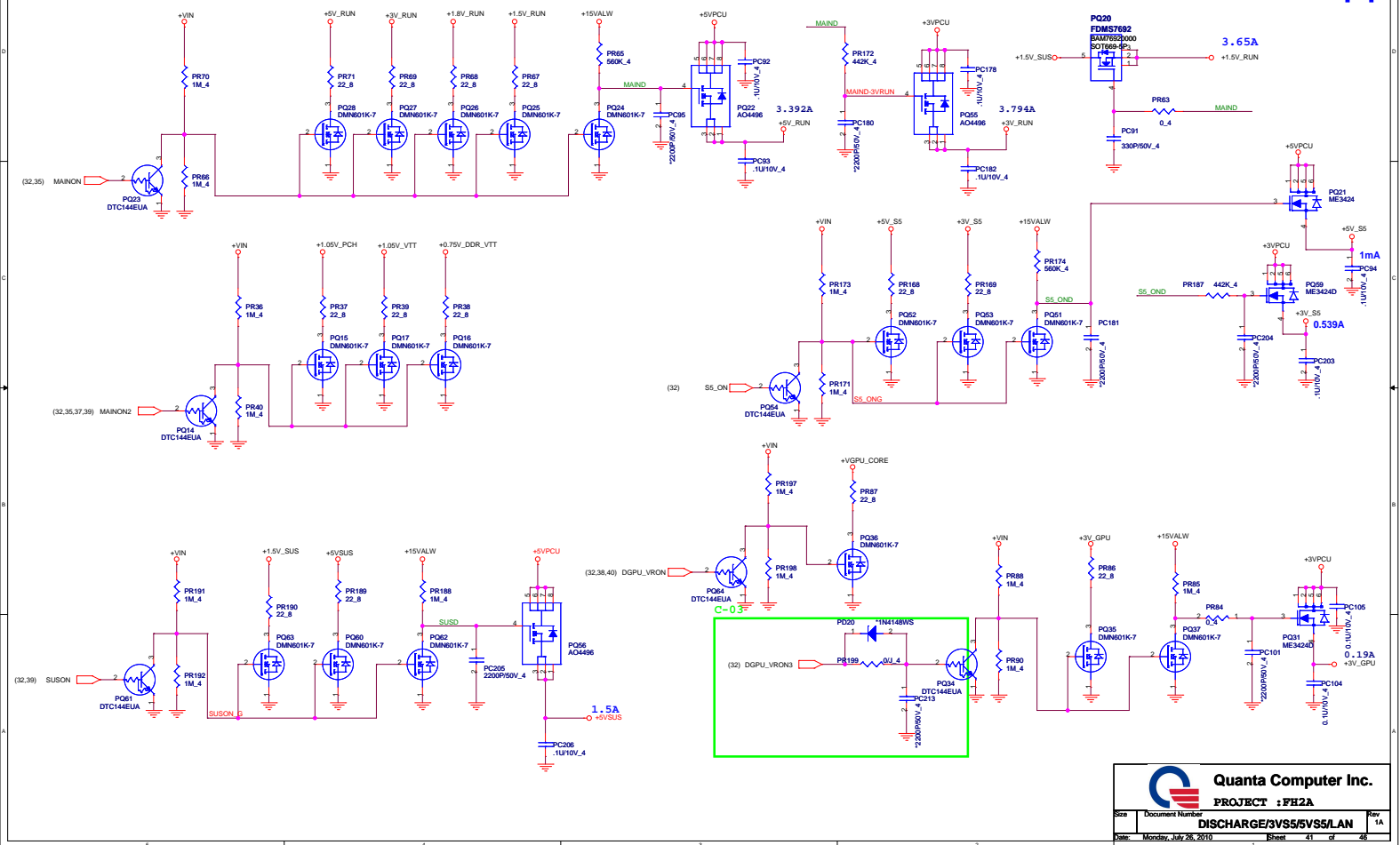


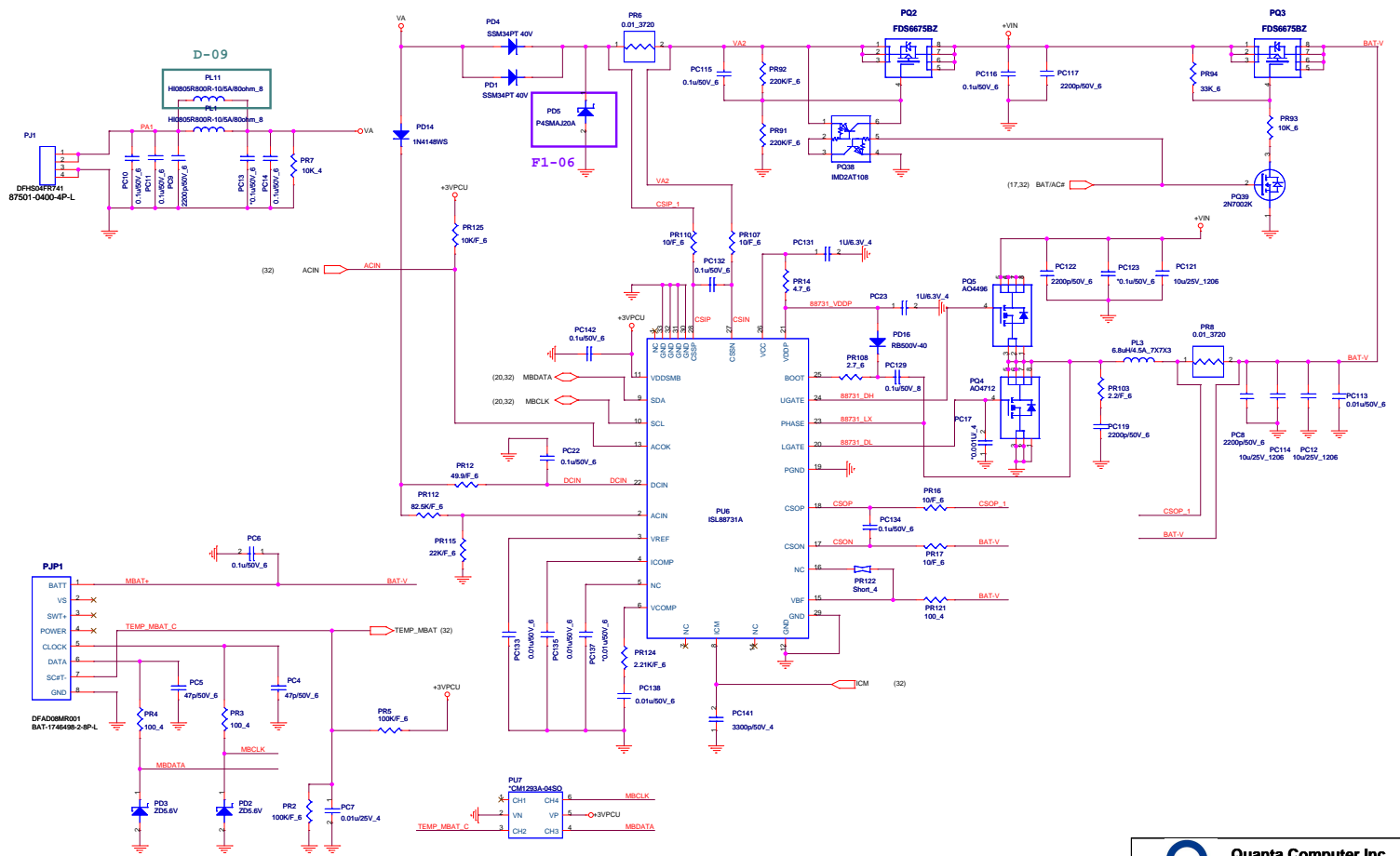


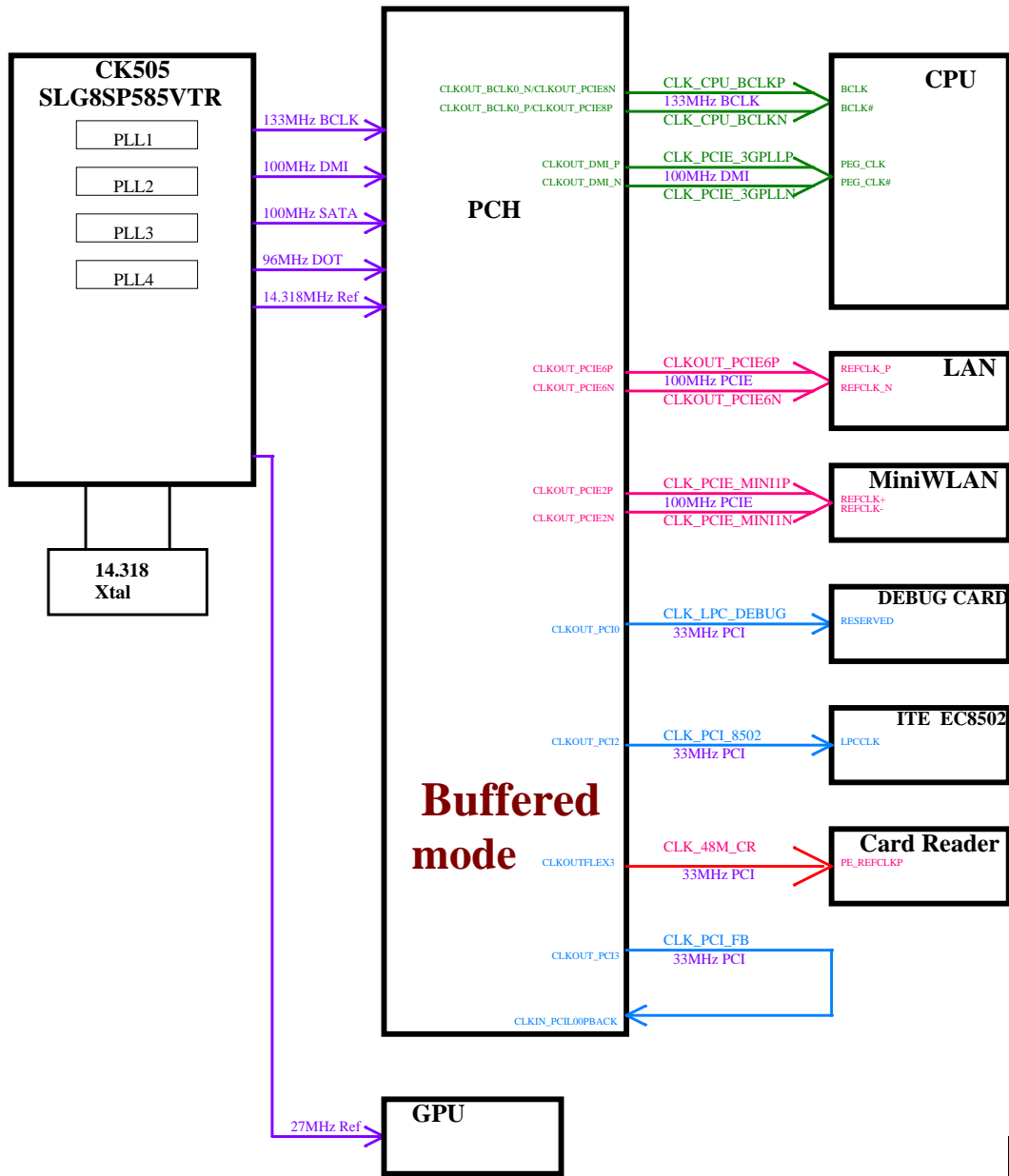
1 Volt +/- 5%  
 Countinue current:2A  
 Peak current:3A

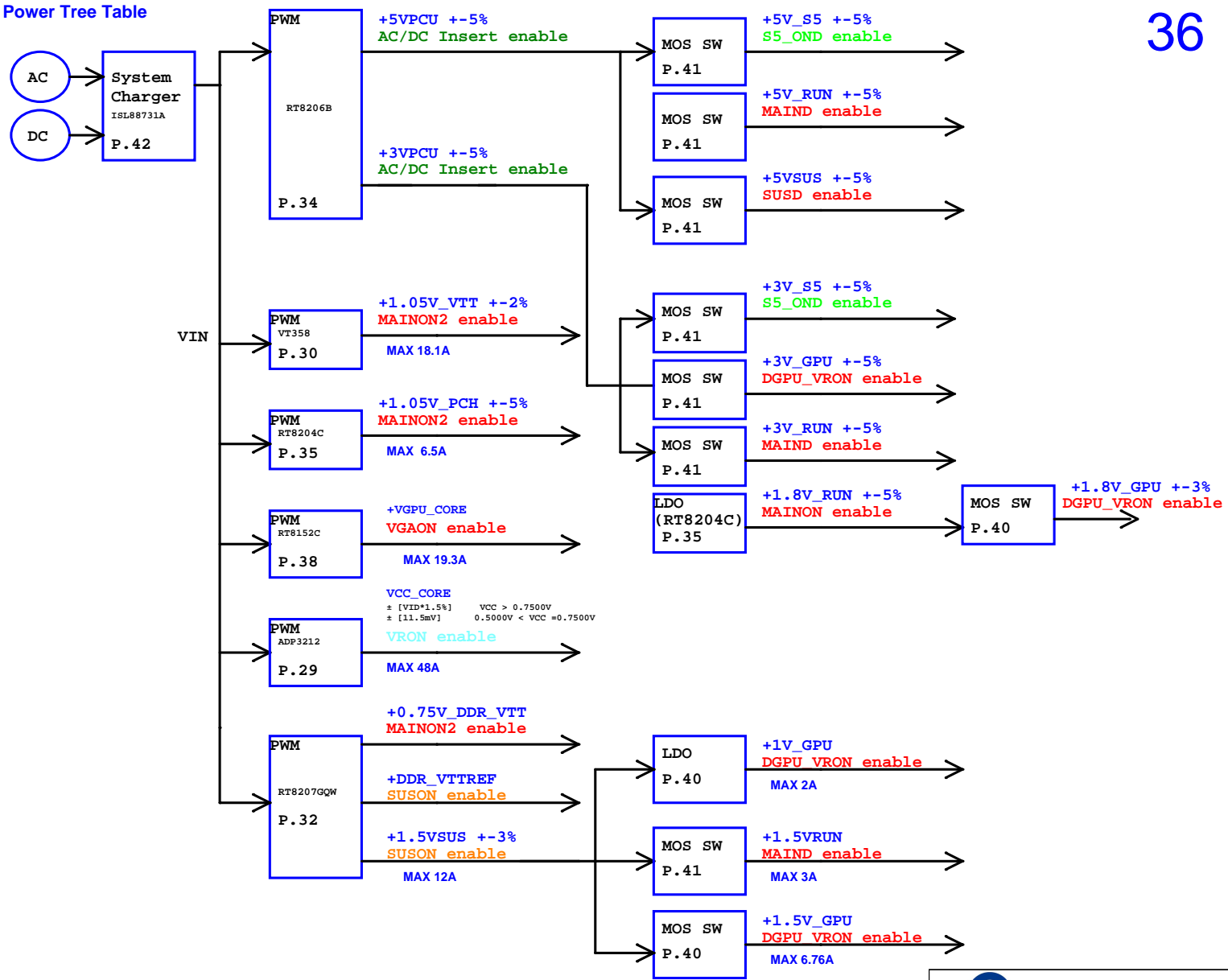


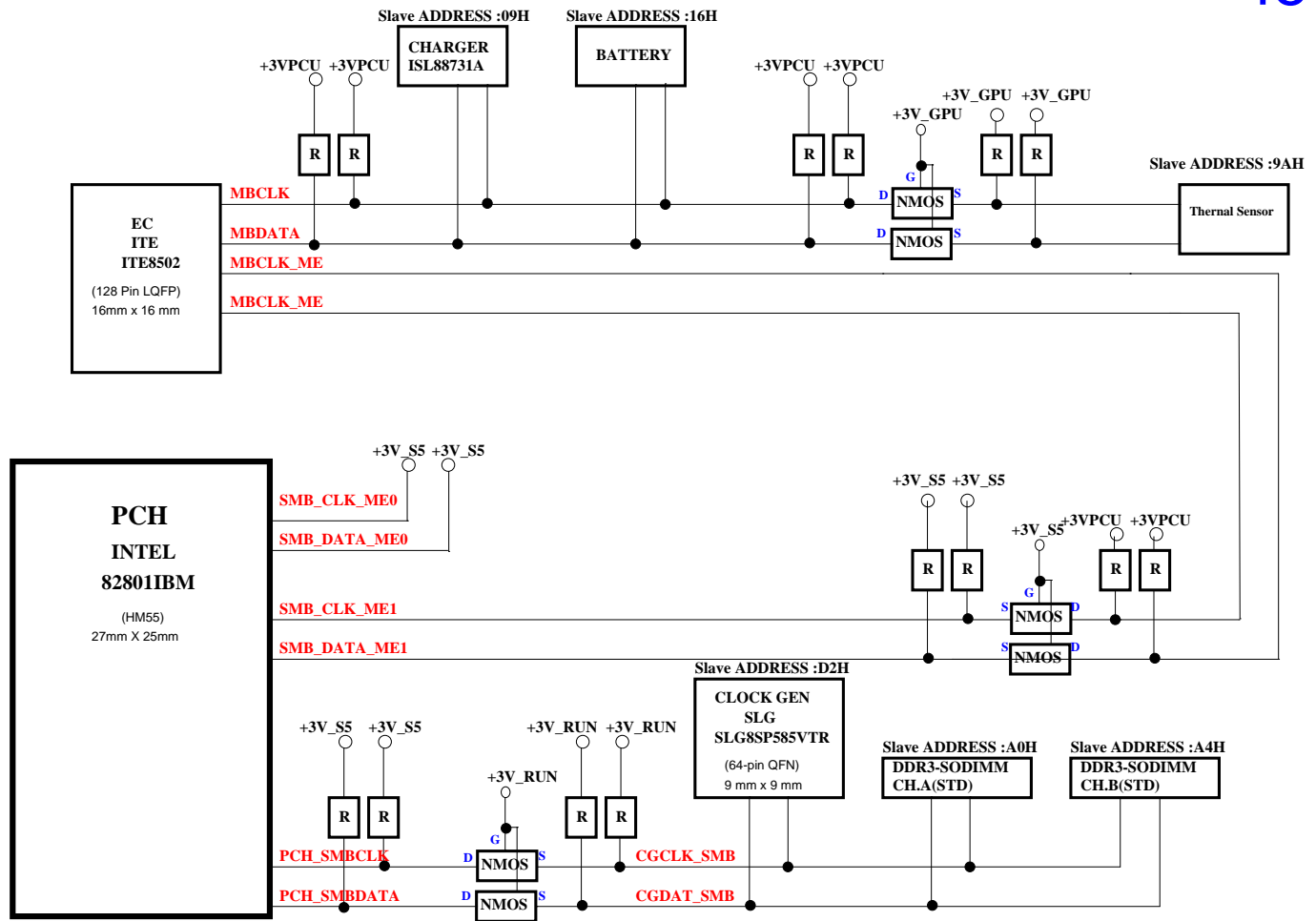












CHANGE HISTORY
<b>A-&gt;B</b>
PAGE04:Delete Q4,Q3,R170,R171,R159 for cost down
PAGE16:R12 delete it for M96 LP BOM
PAGE17:R297-300 can select GPU BOM type for VRAM strap
PAGE18:<1>Add L43,L48,R499,R500 for M96 LP BOM
<2>Add L44 for M96 LP BOM
<3>Add R498 for M96 LP BOM
<3>Delete L26,L10,C199,C200,C208,C23,C39 for M96 LP BOM
PAGE19:<1>Delete L45-47,L12,C42,C36,C29 for M96 LP BOM
<2>Delete R498,R497 for M96 LP BOM
PAGE20:Delete R74,R300,R84,R64,R48 for M96 LP BOM
PAGE28:Delete Q24,C663,Add Q68,Q69,Q26,C708-710,R277,R791 for B/T power control cost down.
PAGE32:Delete R234,Add R229 for BID for RevB.
PAGE34:<1>Increase PC207 10uF/25V 1206 for +5VPCU stable.
<2>Change PR58 from 200k ohm to 150K ohm for OCP function.
PAGE38:<1>Increase PC210(390u2.5V_R6_10), PC211(100uF_3V_8) & PC212(10U/6.3V_8) for +VGPU_CORE stable.
<2>Change PR74 from 15k ohm to 88.7K ohm for Voltage selected function.
<3>Change PR82 from 5.6k ohm to 6.19K ohm for OCP function.
PAGE39:<1>Increase PC208(10U/25V_1206) & PC209(10U/25V_1206) for +1.5V_SUS stable.
<2>Change PR183 from 10K ohm to 18K ohm and PR184 from 10K ohm to 18.7K ohm for Voltage level modification.
PAGE40:<1>Change PR19 from 25.5K ohm to 30.1K ohm for Voltage level modification.
<b>B-&gt;C</b>
PAGE20:<C-01>R81,R83,R54,R51 change to 100ohm for M96 LP DDR3 reference voltage.
PAGE20:<C-02>Delete AR14,AU1,AU2,AC24,R278 for POP noise& add AR13 0ohm & add AD1.
PAGE31:<C-03>Change PR127 to 3.01K for M96 LP power sequence.
Change PR136 to 0 ohm&Delete PC46 for M96 LP power sequence.
Delete PD20,PC213&Change PR199 to 0 ohm for M96 LP power sequence.
PAGE40:<C-04>Add PR203,PR204 100k ohm.
<C-05>Delete C330,C482.
PAGE10/Z8:<C-06> Change PL2 from 0.56uH to 0.88uH&Delete PC3&Add PC96 for VGA CORE power quality.
PAGE38:<C-06> Change PL2 from 0.56uH to 0.88uH&Delete PC3&Add PC96 for VGA CORE power quality.
<b>C-&gt;D</b>
PAGE23:<D-01> Delete U22 & Add R501(CS00002JB38).
PAGE31:<D-02> AMP_PD# circuit change for current leakage issue.
1.Delete AD1,AD2&Add Q24,Q25,Q27(BAM70020001),AR27(CS00002JB38),R189(CS24702JB38).
PAGE38:<D-03> Change PR179 to 3.01K(CS23012FB16).
PAGE34:<D-04> Delete PR176 & PR167.
PAGE35:<D-05> Delete PR35.
PAGE37:<D-06> Delete PR56.
PAGE39:<D-07> Delete PR175.
PAGE40:<D-08> Delete PR123 & PR128.
PAGE42:<D-09> Add PL11.
PAGE39:<D-10> Change PU14 from RT9207A to UP6163AQAG for shortage.
PAGE24:<D-11>Delete D5,R210,R205&Add Q5,Q6(BAM70020001),R203,R206(CS31002JB28) for HDMI 7-13 issue.
PAGE38:<D-12> Add PD13 & PD15 to save power.
PAGE23/31:<D-13> Add AC12,AC13,C503,C504 for EMI
PAGE 31:<D-14> Add de-pop noise circuit.
<b>D-&gt;E</b>
<E-01> For ATI DIAG fail issue.
PAGE 17:<E-01>Change R302 from CS11002FB22 to CS06192FB02.
PAGE 17:<E-01>Change R303 from P/N CS11622FB15 to P/N CS07502FB17.
<E-01>Delete R304(Change to short pad)
PAGE 17:<E-01>Delete R199(Change to short pad)
<E-02> For VGA power sequence re-tuning.
PAGE 38:<E-02>Delete PC225 P/N CH4222K9B04.
PAGE 38:<E-02>Change PR PR226 from P/N CS23012FB16 to CS00002JB38
PAGE 40:<E-02>Change PR200 from P/N CS00002JB38 to P/N CS31402FB12.
PAGE 40:<E-02>Add PC214 P/N CH4222K9B04.
<E-03> For VGA power ripple reduction.
PAGE 38:<E-02>Change PR242 from CS36652FB16 to CS36802FB00.
<b>E-&gt;F</b>
<F-01> For OS hang up issue
PAGE 34,36,40:<F-01>Add C720, C721, C723, C725, C728&C524 change to 1uF
PAGE 36,40:<F-01>Add C722, C724, C726&C728 change to 0.1uF
PAGE 40:<F-01>Add PC210 1uI(0402) for +1.8V_GPU.
PAGE 16:<F-02>Add 0ohm for R49.
<F-03> Reduce 27Mhz for overshoot.
PAGE 17:<F-03>Change R304 to 33ohm from 6ohm.
<F-04> EMI suggestion.
PAGE 23:<F-04>Add L2 for USB common choke.
PAGE 09:<F-04>Add CS92 22P.
PAGE 38:<F-04>Add PC218 2200P & PR123 2.2R.
PAGE 25:<F-04>Add C460 22P.
PAGE 31:<F-04>Add AC5 10P.
PAGE 17:<F-05>Delete D20.
<F-06> PAGE 42: Add PD5 to prevent from surge voltage.